Customer No. 22,852
Attorney Docket No. 04173.0441

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
Hisashi KANEKO, et al.	Group Art Unit:
Application No.: Not Yet Assigned	Examiner:
Filed: January 15, 2004	
For: SIMULATION CIRCUIT PATTERN EVALUATION METHOD, MANUFACTURING METHOD OF SEMI-CONDUCTOR INTEGRATED CIRCUIT, TEST SUBSTRATE, AND TEST SUBSTRATE GROUP	

MAIL STOP - PATENT APPLICATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. § 1.97(b)

Pursuant to 37 C.F.R. §§1.56 and 1.97(b), applicants bring to the Examiner's attention the documents listed on attached Form PTO-1449. Copies of the listed documents are attached. Applicants respectfully request that the Examiner consider the documents listed on attached Form PTO-1449 and indicate that they were considered by making an appropriate notation on this form.

This Information Disclosure Statement is being filed with the above-referenced application.

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The following is a concise statement of relevance of the non-English language document:

1. Japanese patent laid open application no. 2001-44285, discloses a pattern layout method for semiconductor LSI in order to obtain effective information from a test chip by minimizing the difference between the test chip and a product chip. The relevance of this document is also discussed at page 2 of the specification of the present application.

This submission does not represent that a search has been made or that no better art exists and does not constitute an admission that each or all of the listed documents are material or constitute "prior art." If the Examiner applies any of the documents as prior art against any claim in the application and applicants determine that the cited documents do not constitute "prior art" under United States law, applicants reserve the right to present to the office the relevant facts and law regarding the appropriate status of such documents. Applicants further reserve the right to take appropriate action to establish the patentability of the disclosed invention over the listed documents, should one or more of the documents be applied against the claims of the present application.

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If there is any fee due in connection with the filing of this Statement, please charge the fee to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, L.L.P.

Dated: January 15, 2004

By: _____
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Enclosures
RVB/FPD/blc

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OMB No. 0651-0011

INFORMATION DISCLOSURE CITATION

Atty. Docket No.	04173.0441	Application No.	
Applicant	Hisashi KANEKO, et al.		
Filing Date	January 15, 2004	Group:	

U.S. PATENT DOCUMENTS

Examiner Initial*		Document Number	Issue Date	Name	Class	Sub Class	Filing Date If Appropriate
		6,040,912	Mar. 21, 2000	Zika et al.			

FOREIGN PATENT DOCUMENTS

		Document Number	Publication Date	Country	Class	Sub Class	Translation Yes or No
		2001-44285	02/16/2001	Japan			Abstract

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

Examiner	Date Considered

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form PTO 1449 — Patent and Trademark Office - U.S. Department of Commerce